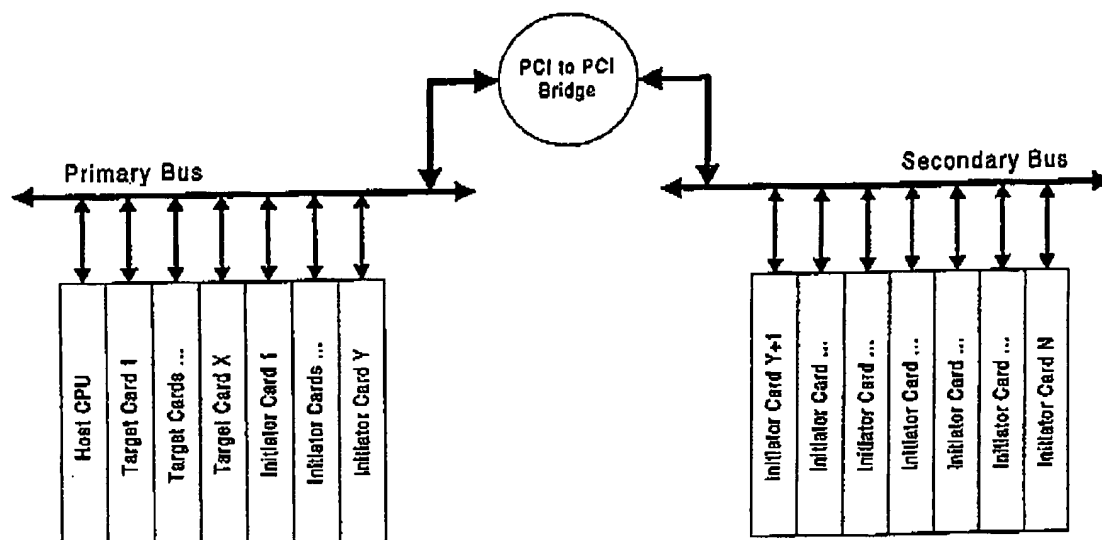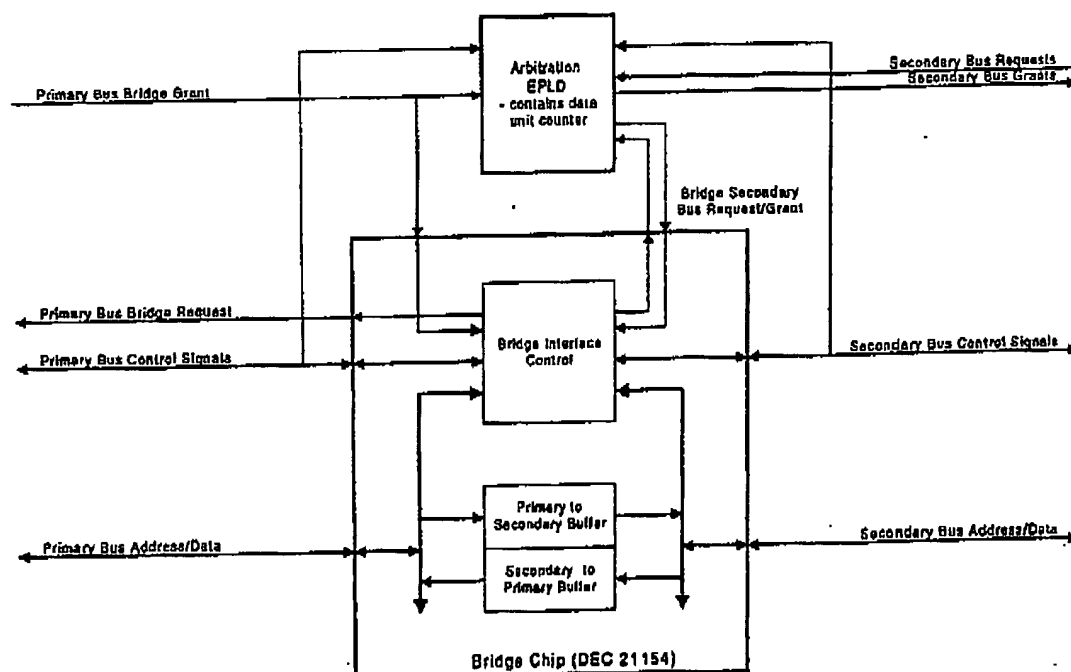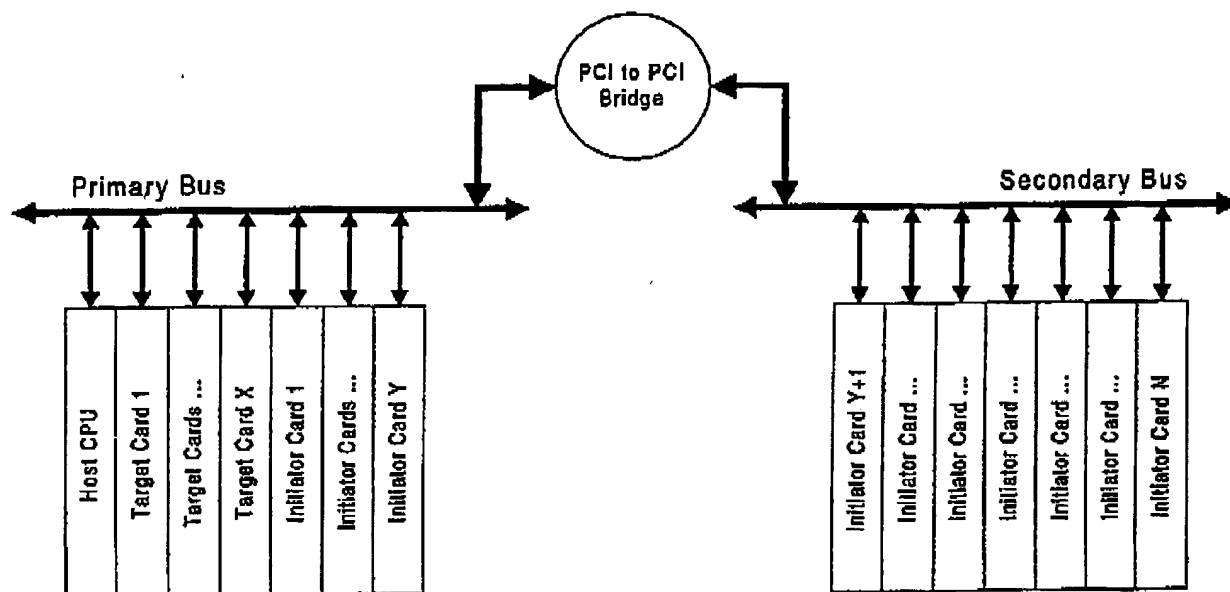Exhibit "B"

BWA Compact PCI Architecture with Host CPU, X Target Cards and N Initiator Cards:

Architecture of PCI to PCI Bridge module using the method described in the invention disclosure form:

Exhibit "B"

BWA Compact PCI Architecture with Host CPU, X Target Cards and N Initiator Cards:

PCI to PCI Bridge

Primary Bus

Host CPU | Target Card 1 | Target Cards ... | Target Card X | Initiator Card 1 | Initiator Cards ... | Initiator Card Y

Secondary Bus

Initiator Card Y+1 | Initiator Card ... | Initiator Card ... | Initiator Card ... | Initiator Card ... | Initiator Card ... | Initiator Card N

Architecture of PCI to PCI Bridge module using the method described in the invention disclosure form:

Arbitration EPLD
- contains data unit counter

Primary Bus Bridge Grant

Secondary Bus Requests
Secondary Bus Grants

Bridge Secondary Bus Request/Grant

Primary Bus Bridge Request

Bridge Interface Control

Primary Bus Control Signals

Secondary Bus Control Signals

Primary to Secondary Buffer

Secondary to Primary Buffer

Primary Bus Address/Data

Secondary Bus Address/Data

Bridge Chip (DEC 21154)